Remarks

In the specification, paragraph [0001] has been amended to include the serial number of the related application.

Further, in the specification, the examiner indicated that Figure 6, Number 608 was not referenced in the specification. The examiner recommended a proposed drawing change or amendment to the specification. Applicant has amended paragraph [0050] of the specification to specifically recite block 608, as the text in this paragraph corresponds to the text at block 608. No new matter has been added by this reference.

Claims 1-39 are pending in the present application. By this amendment, claims 8, and 33-36 have been canceled, and claims 1, 9, 10, 13, 16, 18, 25, 26, and 27 have been amended. Thus, claims 1-7, 9-32, and 37-39 remain.

Before a claim by claim analysis is provided, a brief overview of the art cited by the examiner is considered helpful.

With respect to US Patent No. 5,371,872 to Larsen et al. (Larsen), this patent is directed to an interrupt controller, in conjunction with a cache memory controller, which can be set to prevent or allow use of the cache for different interrupts. Referring to Figure 2 of Larsen, an interrupt controller 28 is provided, along with a cache controller 30. The interrupt controller 28 has external interrupt signals 28, and internal interrupt signals 26. The examiner points this out when he references Larsen, Col. 5, lines 57-60 and 60-63. In addition, the interrupt controller 28 is coupled to a program status vector register 32. Applicant understands the program status register 32 to provide status information 36, relating to interrupts, for information in the cache. The status information is particularly shown in Figure 3. The status information lets the interrupt controller 28 know, for a particular interrupt, whether information related to the interrupt can be fetched from main memory, or the cache, whether the information can be locked or not locked in the cache, and whether data related to the interrupt can be placed in the cache. It appears from Larsen (see Col. 6, lines 28-31) that for each particular interrupt level [which applicant presumes is predefined], a series of program status words 34a-34n are stored to provide program status for a particular interrupt level. Thus, a first interrupt level would have a first program status word 34a, a second interrupt level would have a second program

status word 34b, etc., where each program status word would indicate whether an interrupt at that level could use the cache, and to what extent it could use the cache. This is explained at Col. 7, lines 34-38. Thus, Larsen is interested in taking pre-existing interrupt levels, and coupling them to a cache controller so that the user can define how each interrupt level can use the cache.

In contrast, applicant's invention is not associating pre-existing interrupt levels with cache use. Rather, applicant's invention is directed at allowing a programmer to specify new interrupt levels within a pre-existing architecture, and define target vectors for these interrupt levels, to allow modifiable interrupt handling, including the time required to service an interrupt, for the new intermediate interrupts.

With respect to US Patent No. 6,332,181 to Bossen et al. (Bossen), this patent is directed to a method and apparatus to treat parity errors in a cache from causing a computer system from rebooting. The method used in Bossen is to treat a parity error in a cache as a particular kind of interrupt (a DSI) which can be serviced by a interrupt handler. Applicant notes that nothing in Bossen is directed at creating new interrupt levels, or defining new interrupt levels within pre-existing interrupt levels, or programmably defining or altering priority levels for new interrupt levels. Rather, Bossen is simply using a pre-existing interrupt when a parity error occurs in his cache. The examiner notes Col. 3, lines 60-61 as if such taught that different priorities can be assigned to different interrupts. Applicant respectfully notes that interrupt controllers have typically allowed predefined interrupt signals to have different priorities. These differing priorities are provided on different interrupt request lines, which are built into the computer's internal hardware, and are used to send interrupts to the CPU. See Col. 3, lines 61-62. What is not taught in Bossen, is the ability to define intermediate interrupt levels within a pre-defined architecture, and programmably define interrupt priorities to these interrupt levels. Nothing in Bossen teaches, suggests, or even hints at this novel feature. Bossen simply takes a pre-existing interrupt, and uses it for parity errors in a cache.

With respect to US Patent No. 4,056,847 to Marcantonio, what is described is an way to take multiple interrupt signals 12, latch or store which one of them is active in a storage latch 14, and provide the interrupt signals 12 to an encoder 15. The encoder 15

prioritizes the received interrupt signals 12, and provides just one of them to the processor. This is because, at the time of Marcantonio, processors had a single interrupt line. What is shown in Marcantonio is a more primitive version of what applicant described with respect to his Figure 1 (Prior art). That is, multiple external interrupt signals 12 are input into an interrupt controller, which, according to a predefined priority, provides them to a processor. Applicant is unsure why the examiner cites Marcantonio, except for the fact that he shows a priority encoder for encoding priorities to interrupts. But, as applicant has said, coding of priorities to pre-existing interrupts is not new, and was shown in applicant's Figure 1.

With the above general background on Larsen, Bossen, and Marcantonio, applicant believes that enough general understanding of these references is given to undertake an analysis of the pending claims.

CLAIM REJECTIONS - 35 USC §101

The examiner rejected claims 37, 38 and 39 under 35 USC §101, because the claimed invention is directed at non-statutory subject matter. The examiner stated that claims 37, 38, 39 are directed to an intangible signal because the computer data signal is not contained on a tangible medium. Applicant respectfully traverses.

Applicant commends the Examiner on his original thinking. Although applicant disagrees with the examiner for the reasons that follow, raising such an issue provides the applicant with an opportunity to think thru the rejection and respond accordingly.

By way of background, Applicant prosecuted numerous applications in the late '80's and early '90's where computer programs, computer program code, computer readable program code was held by the patent office as non-statutory under 35 USC §101 because it was not a process, machine, manufacture or composition of matter. In applicant's opinion, such rejections were a result of the law lagging behind technology. A sprinkling of opinions came down which attempted to support the notion that data structures, processes, computer program code, etc., were statutory if embodied in a "physical" medium. (e.g., In re Lowry, 32 F.3d 1579, In re Warmerdam, 33 F.3d 1354). Finally, the Commissioner of the patent office declared "that computer programs embodied in a tangible medium, such as floppy diskettes, are patentable subject matter under 35 USC

Section 101 and must be examined under 35 USC §§102 and 103." In re Beauregard, 35 USPQ2d 1383, 1384 (Fed. Cir. 1995).

So, from applicant's perspective, the issue of whether computer readable program code is proper subject matter, if "embodied in a tangible medium", under 35 USC §101 has already been answered, and answered in the affirmative. Computer readable program code embodied in a tangible medium is patentable subject matter under 35 USC §101. Thus, from applicant's perspective, the issue raised by the examiner is whether such program code in the form of a computer data signal embodied in a transmission medium is a "tangible medium" such as floppy diskettes. That is, is the "such as" language of Beauregard meant to include computer data signals in a transmission medium. Applicant submits that it is.

What is meant by "tangible medium"? Let's trace the path of the computer program code from the floppy disk, through a computer. If computer readable program code is patentable on the floppy disk, is it no less patentable as it is being read magnetically by the floppy disk drive, and communicated over a period of time, via computer data signals (in this case on an ISA cable) to memory? Once it arrives in memory, it is patentable according to In re Lowry. Do you believe that the program code is patentable when on the floppy disk, and when it is in memory, but not when it is in buffers between the floppy disk and the DMA controller, or as data signals on the ISA cable? What is the difference between high and low voltages (or states) in memory, and high and low voltages on an ISA cable? Both can be read by a computer. And, what is the tangible medium in memory? It is certainly not fixed. In fact, if the memory does not get strobed every 80ms or so, the code in the memory will be lost. But, as long as it is in memory, it is patentable. What if some of the code is in memory, and some on a hard disk. Isn't the entire code located in a readable tangible medium? Applicant respectfully submits that if the computer program code is readable by a computer, it is defacto in a tangible medium.

As an example of a transmission medium, Applicant submits that the ISA cable between the floppy disk drive and the ISA bus on the southbridge chip in the computer is a transmission medium. Applicant further submits that other data signal paths within a computer such as IDE, ATA, SATA, PCI, PCI-Express, are all transmission mediums

that contain and/or transfer the computer program code. If you want to know what code is on a transmission medium, it can be monitored, just as if you were reading the code off a hard disk. Other transmission mediums include connections between computers (e.g., Ethernet), and/or connections between computers and storage systems (e.g., Fibre Channel).

One particular connection on an Ethernet transmission medium is a network interface controller. Applicant respectfully submits that computer readable program code is fixed in a tangible "readable" medium when it is located within the fifo's of a network interface controller, since fifo's are just a different type of memory. If this is true, when a data packet is translated from a logical structure in the fifo [which is by case law a tangible medium since a fifo is just a form of memory], into physical voltages, are they no less tangible? At any static point in time, such voltages are observable as an instance of a data signal. And, over a period of time, just like reading program code off a floppy disk drive, code is readable over a network transmission medium. If it were not, then computers such as those used in the patent office, could not be networked. Thus, Applicant submits that whether high/low voltages which describe computer program code are resident in memory, on a hard disk, or on a wire, they are nonetheless tangible and readable. For these reasons applicant submits that program code transmitted via a computer data signal embodied in a transmission medium is a readable tangible embodiment, just like a floppy drive, albeit much faster and more easily readable and transferable. It is certainly readable, it is certainly physical, and given the ubiquitous success of computer networking and the internet, its utility is beyond question. Applicant therefore respectfully requests the examiner to withdraw his rejection of claims 37, 38, 39 under 35 USC §101.

CLAIM REJECTIONS - 35 USC §103

The examiner rejected claims 1, 2, 4, 5, 6, 27, 29 and 30 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, and Marcantonio. Applicant respectfully traverses.

First, applicant is unsure whether the examiner intends on combining the references to form his rejection of these claims, or whether he believes that each of the references can be used alone. Applicant reviewed each of these patents, and found no suggestion, or

even hint, for combining the references. The examiner is reminded that "[i]t is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. Th[e] [Federal Circuit] has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fritch, 972 F. 2d 1260, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). Applicant respectfully suggests that different features of the claimed invention from different prior art sources cannot be combined unless the examiner explains the motivation to combine or modify the references. That it "would be obvious" is not an adequate motivation. A specific teaching, or suggestion to make the modification is required. Applicant respectfully suggests that there is no hint or suggestion in any of the three references to combine them. With this in mind, claim 1 is repeated below for ease of reference:

1. (Currently amended) A processing system comprising:

a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;

a plurality of second interrupts that are generated external to said core;

a status register, coupled to said core, having a vector table, and an interrupt register, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities, said programmable priorities being different than those architected for said plurality of second interrupts; and

a priority encoder, coupled to both said first interrupts and to said second interrupts, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities.

Applicant has amended claim 1 to specifically claim what was already implicit in a number of dependent claims. That is, that the programmable priorities of applicant's

invention are programmable, not at time of manufacture, but by the processing system. And, that the programmable priorities are different than those that are "programmed" or "architected" for the processor, for its external interrupts, at the time of manufacture. In contrast to the cited art, applicant provides a mechanism for programmably defining, by the operating system executing on the processing system, intermediate, or different, priority levels for core generated interrupts. This is nowhere taught, suggested, or even hinted at by the cited art.

More specifically, the examiner stated that Larsen teaches a processing system comprising a plurality of first interrupts generated by a core, and a plurality of second interrupts that are generated external to the core. Applicant agrees. The examiner further stated that Larsen does not teach that said plurality of first interrupts have programmable priorities and a priority encoder. Applicant also agrees. The examiner further states that Bossen teaches that different priorities can be assigned to different interrupts. Applicant traverses. Applicant submits that what Bossen teaches, is that he has different interrupt levels that can be assigned to different interrupts. This is not new. But, in Bossen, applicant believes that the interrupt levels are not alterable by the processing system. That is, Bossen may have predefined interrupt levels (e.g., 0, 1, 2, etc.) that may then be assigned to particular interrupts. But, this is different than having the ability to program additional priority levels (e.g., 1.5, 2.5, etc.) that are considered by a priority encoder when handling interrupts. The examiner further states that Marcantonio teaches a priority encoder. Applicant agrees. But, Marcantonio's priority encoder is a hardware structure that can only prioritize architected, or fixed interrupt levels. Marcantonio has no ability to deal with prioritization of non-architected interrupt levels. Further, nothing in Larsen, Bossen, or Marcantonio suggests a combination with each other. And, even if they did, what the combination would teach (speculating), would be a dedicated hardware priority encoder for prioritizing architected interrupt priority levels (from Marcantonio), used to prioritize an interrupt for a cache parity error (from Bossen), where such error included cache status information indicating whether the interrupt handler for the parity error had the ability to use the cache. None of this is directed at the novelty of applicant's invention, as recited in claim 1. For all these reasons, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 2-7, and 9, these depend from claim 1 and add further limitations which are neither anticipated nor obviated by Larsen, Bossen, and/or Marcantonio, taken alone or in combination. For the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner rejected claims 3 and 28 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, and Marcantonio, and further in view of US Patent No. 5,768,500 to Agrawal et al. (Agrawal). Applicant respectfully traverses. Agrawal utilizes a cache miss counter with a compare register and interrupt line such that his processor is interrupted when the counter matches the compare value, so he can sample system state and develop cache miss profiles that associate cache misses with specific processes. procedures, call stacks. addresses, or user defined aspects of system state. That is, he allows a counter to periodically trigger an interrupt to track performance of a cache. In claim 3, applicant indicates that one of his interrupts is a performance counter interrupt. But, this is an additional limitation to what is recited in claim 1, which as mentioned above, is novel over Larsen, Bossen and Marcantonio. Applicant further submits that claim 3, is therefore novel over this combination, in combination with Agrawal. Applicant therefore respectfully requests the examiner to withdraw his rejection of claim 3.

The examiner rejected claims 8 and 9 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, and Marcantonio and further in view of US Patent No. 5,822,595 to Hu et al. (Hu). Applicant respectfully traverses. Applicant has already stated his reasons for traversing the rejection of claim 1. Claim 8 has been canceled which renders the rejection of this claim moot. Claim 9 depends from claim 1 and adds further limitations which are not anticipated by the Larsen, Bossen, Marcantonio combination. Hu adds nothing to this combination. What Hu shows is an interrupt handler unit IHU for polling and arbitrating among interrupt sources (see Abstract). At Col. 3, lines 43-46, Hu teaches that each interrupt source can be programmed to one of four priority levels, via the interrupt priority registers. What this means is, for pre-existing, pre-architected priority levels, interrupts can be assigned to those levels. This is not the same as programming of priority levels. More specifically, Hu is not teaching that new priority levels may be programmed. Rather, he is teaching that existing priority levels may be programmably

assigned to interrupts. This is not the same as what applicant has claimed. For these reasons, as well as those stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

The examiner further rejected claims 10, 11, 12, 13, 14, 22, 23, and 24 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio and Hu. Applicant respectfully traverses.

A brief background of Larsen, Bossen, and Marcantonio was already presented above. And, as mentioned above, Hu teaches that interrupt sources can be programmed to one of four priority levels via interrupt priority registers. Col. 3, lines 43-46. And, as mentioned above, it is not the priority levels that are being programmed in Hu, but the interrupts which are programmably assigned to pre-existing priority levels. With this in mind, claim 10, as amended, is repeated below for ease of reference.

10. (Currently amended) A microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the microprocessor comprising:

a core, for executing instructions, said core generating second interrupts;

priority storage logic coupled to said core, for storing programmable priorities for said second interrupts, said programmable priorities being different than priorities for the first interrupts; and

a priority encoder, coupled to said core, and to said priority storage logic, for receiving the first and said second interrupts, and for prioritizing the first and said second interrupts utilizing said programmable priorities stored in said priority storage logic.

With respect to claim 10, it clearly claims "programmable priorities". That is, unlike Hu, what is being programmed are priorities, or priority levels. This is not the same as programmably assigning existing priorities to interrupts. This was claimed in the original claim 10, and is being repeated in the amended claim.

The examiner states that Larsen teaches a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the microprocessor comprising a core, for executing instructions, said core generating second interrupts. Applicant agrees. The examiner further states that Larsen does not teach priority storage means [logic] for storing programmable priorities ... Applicant also agrees. The examiner further states that Bossen teaches that different priorities can be assigned to different interrupts. Applicant has already disagreed with this above, but no matter, this is not what is being claimed. The examiner further states that Marcantonio teaches a priority encoder. Applicant has responded to this above with respect to claim 1. The examiner further states that Hu teaches a plurality of interrupt priority registers for storing priorities of the interrupt sources. Applicant agrees that Hu teaches such registers for storing pre-existing priorities for interrupt sources. But, as mentioned above, Hu does not teach, nor does Larsen, Bossen, or Marcantonio, taken alone or together, the novel aspect of programming priorities. For this reason, and for all those above, applicant respectfully requests the examiner to withdraw his rejection of claim 10.

With respect to claims 11-26, these claims depend from claim 10 and add further limitations which are neither anticipated nor obviated by Larsen, Bossen, Marcantonio and Hu, taken alone or together. For the reasons stated above with respect to claims 1 and 10, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner further rejected claims 16 and 17 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu, and further in view of US Patent No. 5,664,200 to Barlow et al. (Barlow). Applicant respectfully traverses. Applicant has already responded to rejections based on Larsen, Bossen, Marcantonio, and Hu, taken alone or together. With respect to Barlow, what he teaches is an interrupt system between multiple processors. In Barlow, all of the interrupt levels are pre-existing. The examiner refers to Col. 6, lines 5-11 of Barlow as teaching a means to indicate the level of a corresponding interrupt. Applicant agrees that this is what Barlow teaches, but this is not what is claimed in claim 10. Nowhere is Barlow directed at programming of priority levels or priorities, but rather, of latching, storing, etc., of existing priority levels with interrupts. For this reason, and for all of those stated above

with respect to claims 1 and 10, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner further rejected claims 18 and 19 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu, and further in view of US Patent No. 5,148,544 to Cutler et al. (Cutler). Applicant respectfully traverses. The examiner cites Cutler as teaching that registers for storing information related to an interrupt condition are accessible only during a privileged mode. Perhaps so. But, the interrupt conditions of Cutler (and Larsen, Bossen, Marcantonio, and Hu) are for pre-existing, architected priority levels. Nowhere does any of these references teach programming of priority *levels*, as discussed above with respect to claims 1 and 10. For this reason, and for all of those stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner further rejected claim 20 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu, and further in view of US Patent No. 4,110,822 to Porter et al. (Porter). Applicant respectfully traverses. The examiner cites Porter as teaching that interrupts may be assigned to one of eight priority levels. Col. 9, lines 25-29. Applicant agrees that this is what Porter teaches. Applicant notes that the priority levels in Porter are architected, pre-existing, priority levels. As mentioned above, applicant's invention allows the programming of priority levels, not the programmable assignment of existing priority levels to interrupts. For this reason, and for all those stated above, applicant therefore respectfully requests the examiner to withdraw his rejection of this claim.

The examiner further rejected claim 21 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio, Hu, and Porter, and further in view of US Patent No. 4,402,042 to Guttag et al. (Guttag). The examiner cites Guttag as teaching that a processor can have 16 interrupt levels that can be used for internal interrupts. Applicant agrees that this is what Guttag teaches. But, these are pre-existing, architected, interrupt levels, NOT programmed interrupt levels. For this reason, and for all of those stated above, applicant respectfully requests the examiner to withdraw his rejection of this claim.

The examiner further rejected claims 25 and 26 under 35 USC §103(a) as being unpatentable over Larsen, Bossen, Marcantonio and Hu, and further in view of US Patent No. 5,940,587 to Zimmer. The examiner cites Zimmer as teaching a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector. Col. 3, lines 30-41. What Zimmer teaches in this location is a table featuring a plurality of entries corresponding to an interrupt, the entries each having a trap address which includes a segment and an offset. However, as mentioned numerous times above, the interrupt is at a pre-existing, architected, priority level. This is different than what is claimed in claim 10 from which these claims depend. For the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 27, it is repeated below, as amended, for ease of reference.

27. (Currently amended) A method for prioritizing on-core and off-core interrupts within a processing system, comprising:

receiving the off-core interrupts;

receiving the on-core interrupts, the on-core interrupts having programmable priority levels which are intermediate to priority levels for the off-core interrupts;

sorting the received off-core and on-core interrupts according to their priority levels; and

producing an indication of which of the received off-core and on-core interrupts has the highest priority.

Claim 27 previously recited that the on-core interrupts have programmable priority levels. And, as mentioned above, programmable priority levels means that it is the levels which are programmable, not the association of pre-existing levels to particular interrupts. However, to make this even clearer, applicant has amended claim 27 to specify that the programmable priority levels are intermediate to priority levels for the off-core interrupts

(which might be pre-existing). Such intermediate priority levels is nowhere taught, suggested, or even hinted at by any of the references cited by the examiner. Moreover, the prioritization of interrupts, utilizing the priority levels which were programmed, is nowhere taught by the references cited by the examiner. Applicant recites claim 27 because the examiner has rejected claims 31 and 32, under 35 USC §103(a) as being unpatentable over Larsen, Bossen, and Marcantonio, and further in view of Zimmer. Applicant traverses. Claims 31 and 32 depend from claim 27 and add further limitations which are neither anticipated nor obviated by these references, taken alone or in combination. None of them are addressed at programmable priority levels. For this reason, and for all of those above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner further rejected claim 33 under 35 USC §103(a) as being unpatentable over Larsen and Marcantonio, and further in view of US Patent No. 5,758,096 to Barsky et al. (Barsky). The examiner further rejected claims 34 and 35 under 35 USC §103(a) as being unpatentable over Larsen, Marcantonio, and Barsky, and further in view of Barlow. Applicant has canceled claims 33-36 thereby rendering these rejections moot.

With respect to claims 37-39, they are novel for the same reasons as stated above with respect to claims 1, 10 and 27. With respect to their being statutory, applicant has discussed this already above.

Oath/Declaration

The examiner has indicated that a new oath or declaration is required because the title on the declaration is inaccurate. Applicant is willing to comply with this request, if after the examiner reviews the below, he still considers it necessary.

On October 12, 2001, the present application was filed, under Express Mail, with the US Patent Office without inventor signatures. A copy of the original return postcard is attached to this amendment, as Exhibit A. Approximately two weeks later, applicant received the return postcard, a copy of which is attached at Exhibit B. The serial number given to this case was 09/977,089. However, on the same day, applicant's also filed Serial No. 09/977,084 (MIPS.0140-00-US). Return postcards for these two cases arrived on the same day. Applicant's docketing clerk inadvertently entered the serial numbers

for these two cases, reversed. That is, the serial number for the present case was entered as 09/977,084, and the serial number for MIPS.0140-00-US was entered as 09/977,089.

On November 15, 2001, the Patent Office mailed a Filing Receipt, a copy of which is attached hereto as Exhibit C. The filing receipt correctly shows the title, the serial number, and the docket number for the present case. On the same day, the PTO mailed a notice of missing parts, correctly identifying the present application, a copy of which is attached hereto as Exhibit D. Applicant responded to the notice of missing parts by filing a declaration, as shown in Exhibit E. Please note that this declaration incorrectly specified the serial number to be 09/977,084. On the same day, applicant also responded to a notice of missing parts in MIPS.0140-00-US, with a declaration that showed the docket number to be MIPS.0140-00-US, and the serial number to be that of the present case 09/977,089.

In June of 2002, the swapped serial numbers was discovered. The PTO was contacted, and the attorney for applicant was told that the PTO only examines the serial number, not the docket number, not the title, etc. Thus, the attorney was told that he did not have to correct the matter. However, the attorney believed otherwise, and on June 24, 2002, he filed a supplemental declaration, correctly identifying the serial number, docket number, and title for the present application. A copy of the supplemental declaration is attached hereto as Exhibit F.

Applicant therefore believes that a declaration, which correctly identifies the present application, by serial number, by inventor, by docket number, and by title, is part of the record for this case.

Applicant has made an earnest attempt to respond to each of the examiner's rejections, and believes that by this amendment, that the present case is in condition for allowance.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

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Date: 10-5-04

"EXPRESS MAIL" mailing label number EO002743705US. Date of Deposit 10-5-04. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: Vicki J Hogan